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Schottky barrier modulation using ultrathin MgO for metal–silicon (100) contacts

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In this work, ultrathin MBE-grown MgO has been employed as a thin tunneling interlayer to modulate the Schottky barrier height (SBH) between metal contacts and Si substrates. The ultrathin MgO films were grown with different starting first monolayers (O_2, MgO, and Mg) on Si. With an MgO ultrathin film, all contacts show rectifying behavior for both n- and p-type Si. The SBH generally increases (decreases) with increasing metal work function for n-type (and p-type) and is generally lowest for the oxygen first treatment. To our knowledge it is the first time that the role of the first monolayer of an oxide tunnel barrier on the SBH is revealed. These results indicate a novel, interesting way to modulate the barrier height and hence the contact resistivity in CMOS devices.

1. Introduction

The metal/semiconductor junction is of critical importance for many electrical devices such as spintronics,[1] high power devices[2,3] and tunneling field-effect transistor.[4] For sub-0.1 μm CMOS technology nodes, achieving low metal source and drain (S/D) contact resistivity is becoming very challenging due to Fermi-level pinning at the metal/semiconductor interface.[5] The interface index or the pinning factor S, which is defined as the derivative of the Schottky barrier height (SBH) over metal work function, can be used as an index indicating the degree of Fermi-level pinning.[6] A unity S represents a completely unpinned structure. For metals on covalent materials such as silicon and germanium, S is often much lower than unity. For example, S of silicon was reported to be smaller than 0.2.[7] Moreover, S is shown to have an inverse relationship with the dielectric constant of the material underneath.[8]

The reasons for Fermi-level pinning are often attributed to two theories. The first one is known as the metal-induced gap states (MIGS),[9] which is based on the penetration of metal wave functions into the semiconductor. The tail of the metal wave function causes energy states in the semiconductor bandgap. In the second theory, the surface states are due to bond polarization at the interface.[10] The Fermi level can be pinned at the charge neutrality level, where the surface defect level changes from donor type to acceptor type.

An ultra-thin interface dielectric layer in between the metal and the semiconductor can be a possible solution to de-pin the Fermi-level[11] or modulate the SBH.[12] An ideal interlayer should be thick enough to block the deep states in the semiconductor band gap, but still thin enough to be transparent for carriers. The optimal thickness depends on the materials and processes of contacts, interlayer and semiconductors. Moreover, the material of the interlayer must be stable in contact with both semiconductor and metal.

MgO is a strongly ionic oxide with a medium dielectric constant, and is thermodynamically stable on Si. This stimulated our interest to study the effect of an ultrathin MgO interface layer — with the different interface treatments — on the potential barrier between metal and semiconductor. In this research, ultrathin MgO was employed as a tunneling interlayer to modulate the SBH and the contact resistivity. We have specifically focused on determining the influence of different interface treatments (O_2, MgO, and Mg) on these parameters for films grown on both n- and p-type Si substrates.

2. Experimental methods

N- and p-type silicon (100) wafers doped with $4 \times 10^{14}\,cm^{-3}$ P and $1 \times 10^{15}\,cm^{-3}$ B respectively were used as substrates. The wafers were dipped in 0.5% HF solution for 2 min to remove the native oxide and to form H-terminated surfaces, and then loaded into a vacuum chamber within 5 min. MgO films were deposited using an oxide molecular beam epitaxy (MBE) in an ultra-high vacuum chamber with a base pressure of 2×10^{-9} mbar. Hydrogen desorbed from the Si wafers after heating up to 600 °C for 5 min, leading to a clean and 2×1 reconstructed surface; the Si wafers were then cooled to 360 °C for the growth of MgO films. Mg vapor was evaporated from a thermal Knudsen cell with a flux rate 0.1 Å/s calibrated by a quartz crystal monitor. And molecular oxygen was introduced into the chamber, where it reacted with Mg on the substrate and formed MgO. In order to form the three different initial monolayers, namely O_2 ML, MgO ML, and Mg ML as shown in Fig. 1, the Mg flux and O_2 were introduced at different times. For the O_2 ML, O_2 was introduced 1 min before opening the Mg cell shutter, while for the Mg ML, Mg was deposited for 20 s before introducing O_2. The pressure during growth was 5×10^{-5} mbar. The MgO deposition time to grow a 0.5 nm thin interlayer was estimated to be 50 s. Note that this thickness is just slightly larger than the crystalline MgO unit cell length of 0.42 nm so that at least one unit cell is expected to be present everywhere. The growth temperature of silicon substrate was 360 °C.[13]

Subsequently, the 2-in. silicon wafers with thin MgO interlayers were cut into several pieces, which were then transferred to another MBE system to form the different contacts. The base pressure of the metal MBE is 1×10^{-9} mbar. Various work function metals were used, including Er, Al, Au, and Pt, which, combined with the three interface treatments and the two doping types, resulted in 24 different samples. In each case, 40-nm-thick metal pads of different sizes were deposited onto the samples through a shadow mask. The deposition rate was 0.1 Å/s, and the substrates were kept at room temperature.

The samples were attached to a copper plate with conducting glue as back contact. Electrical current–voltage (I–V) characterization was then performed with a Keithley 4200-SCS. $40 \times 40\,\mu m^2$ pads were used in all measurements. Voltage was applied on the top contacts, and the bottom contacts were grounded. For all these samples the SBH and the ideality factor was extracted from I–V curves.

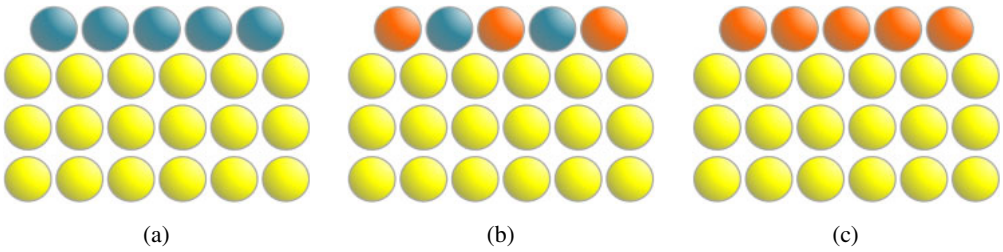

Fig. 1. (Color online) Scheme of the three initial monolayers of MgO on Si: (a) O_2 ML, (b) MgO ML, and (c) Mg ML. Yellow circles represent silicon atoms. Blue and orange ones are oxygen and magnesium respectively.

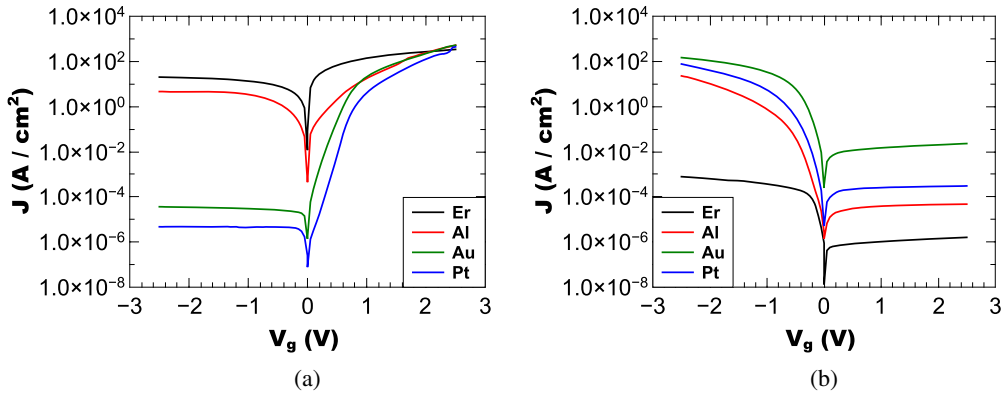

Fig. 2. (Color online) *I–V* curves of different metal contacts with an ultrathin MgO interlayer with O_2 ML treatment on (a) n-Si and (b) p-Si.

3. Results and discussion

3.1 Results

I–V curves for the different metal contacts on n- and p-type Si with the O_2 ML interface are shown in Fig. 2. All *I–V* curves are rectifying, which indicates that the barrier for majority carriers to flow from metal to semiconductor is higher than from semiconductor to metal. The deviation of log *I–V* curves from linearity may be due to the series resistance or the non-uniform barrier height over the contact area.[14] The *I–V* curves in Fig. 2(a) show a clear decrease of the reverse bias current with increasing metal work function. A weaker dependence on metal work function is found for p-Si samples.

Moderate doped Si wafers are necessary for this research in order to suppress the tunnelling current through the barrier. This allows SBH extraction from mainly thermionic emission current. The ideal current and voltage relationship of the thermionic emission mechanism follows from

$$I = AA^*T^2e^{-q\Phi_B/kT}(e^{qV/nkT} - 1), \quad (1)$$

where I is the current, A the contact area, A^* the Richardson constant (112 and 32 $A\cdot cm^{-2}\cdot K^{-2}$ for n- and p-type Si[15] respectively), T the temperature, q the electron charge, Φ_B the effective barrier height, k the Boltzmann's constant, V the voltage, and n the ideality factor.

Figure 3 shows an example of a semilog plot I versus V and the fitting of these curves. In the forward bias region, for voltages higher than $3kT/q$ but still low enough to limit the influence from the series resistance, the log I is linear proportional to V. The SBH Φ_B and the ideality factor n can then be extracted from the y-intercept. For each structure,

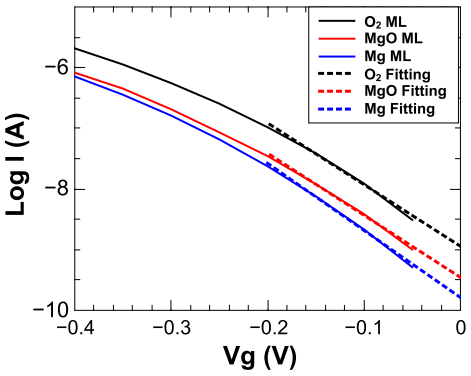

Fig. 3. (Color online) Linear fitting of the *I–V* curves of Pt contacts on p-Si at low forward bias. The SBH is extracted from the y-intercept, and the ideality factor n is calculated from the slope.

three devices were measured; the error of the extracted SBH is within ±1.5% for all samples. From plotting these data it is immediately clear that the O_2 ML interface has the larger intercept and thus the smaller barrier. This trend was obtained for nearly all the systems reported in this study.

The extracted SBH values were listed and compared with the metal work function[16] in Tables I and II for n-Si and p-Si respectively. Among the metals, lower (higher) work function metals generally lead to lower barrier height for n-type (p-type) Si. Surprisingly, among the different interfacial monolayers, the O_2 ML interface generally has the lowest SBH among the three for both n-Si and p-Si. The rare earth metal Er leads to the lowest SBH of 0.39 eV on n-Si with O_2 ML MgO. The ideality factors are generally between 1 and 2.

Table I. Barrier height extracted from *I–V* and metal work function of contacts on n-Si.

Metal	Work function (eV)	Barrier height (eV)		
		O_2 ML	MgO ML	Mg ML
Er	3.09	0.39	0.56	0.49
Al	4.16	0.51	0.6	0.59
Au	5.29	0.71	0.81	0.83
Pt	5.53	0.8	0.82	0.84

Table II. Barrier height extracted from *I–V* and metal work function of contacts on p-Si.

Metal	Work function (eV)	Barrier height (eV)		
		O_2 ML	MgO ML	Mg ML
Er	3.09	0.74	0.71	0.72
Al	4.16	0.69	0.63	0.67
Au	5.29	0.54	0.62	0.58
Pt	5.53	0.64	0.67	0.69

We found that a more reactive metal, such as Er, leads to higher and more dispersed *n* than less reactive metals, such as Pt and Au. This can be either due to the reaction between metal and MgO or the oxidation of the metal. Nevertheless, even for these samples our main observation remains valid, namely that the O_2 ML MgO layer leads to lower SBH. On a few samples, complimentary capacitance–voltage (*C–V*) and temperature-dependent *I–V* curves were performed, which also support the same conclusion.

The SBH versus metal work function data are summarized in Fig. 4. As can be expected from the *I–V* curves, the SBH of contacts on n-Si has a stronger dependence on the metal work function than on p-Si. This suggests that the degree of Fermi-level pinning is smaller in n-type than p-type Si. The interface index *S* can be obtained from the slopes of the linear fitting curves in Fig. 4. The interface index ranges from 0.11 to 0.16 for n-Si, while for p-Si *S* is smaller than 0.1 for all three treatments. Note that linear fitting curves of samples with the O_2 ML are the steepest, which indicates a higher *S* among the three treatments for both n- and p-type Si.

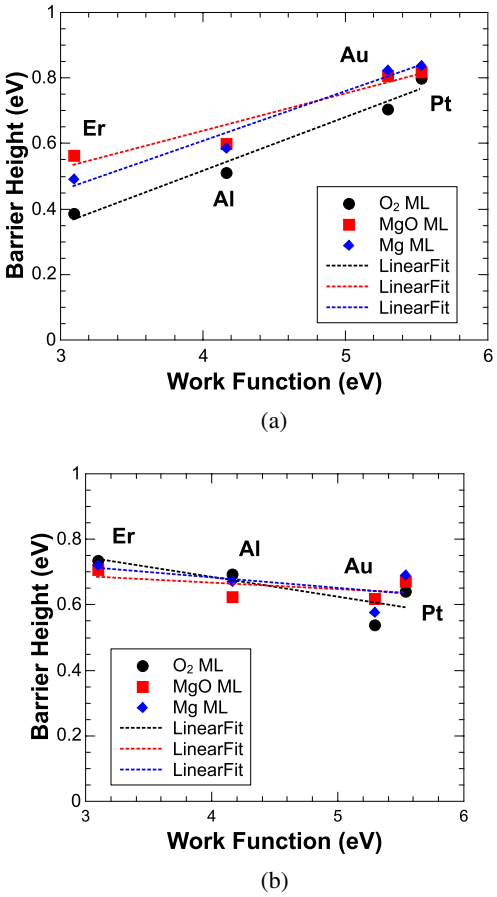

Fig. 4. (Color online) Barrier height versus metal work function plot with three different interface treatments: (a) n-Si and (b) p-Si. The dotted lines show the linear fitting of each curve.

3.2 Discussion

Why do n- and p-Si possess such a difference in the degree of Fermi-level pinning, i.e., different interface indexes between two types of substrates? And what causes the lowest SBH and the steepest fitting slopes of O_2 ML samples for both types of wafers? In the following paragraphs we list a number of contributing factors.

Recently we showed[17] that for MOS capacitors composed of 5 nm MgO on Si, the O_2 ML first treatment leads to a more negative flatband voltage shift in capacitance versus voltage curves due to a higher density of positively charged oxygen vacancies compared to the other treatments. In addition, the O_2 ML causes the lowest D_{it}. These two observations suggest that the Fermi-level pinning can be tailored in this manner. Lin et al.[18] have calculated the barrier height of metal contacts on Si with thin dielectric interlayers. They found that changing the oxygen density in the cells close to the interface can lead to a difference in the barrier height of up to 0.5 eV. The effect of fixed charges was presented by Hu et al.[19] Their results suggest that positive charges in the thin dielectric layer increase the potential drop in the interlayer, and thus reduce the depletion width in the semiconductor and the SBH.

The degree of Fermi-level pinning can also be influenced by dipoles formed at the interface. Considering different bonding between the oxide and silicon for the different initial monolayers, since the Pauling electronegativity of O and Mg are 3.44 and 1.31, and the ion radii of O^{-2} and Mg^{+2} are 0.14 and 0.066 nm[20] respectively, larger dipole moments can be expected for the O_2 ML samples. This difference can then provide the driving force for the Fermi-level de-pinning of the O_2 ML structures.

Another factor is the thickness of the interlayer. Note that an accurate thickness measurement after the growth is very challenging and beyond the resolution limit of most techniques. Furthermore, if we consider the different initial processes during interlayer formation, the O_2 introduction prior to MgO deposition for O_2 ML samples may lead to a slightly thicker silicon sub-oxide layer. The thicker overall interlayer can further block the penetration of metal wave functions into the semiconductor, thus reducing the SBH and the level of Fermi-level pinning.

A similar SBH asymmetry between n- and p-type Ge has previously been observed in the literature.[21] Ge is known for strong Fermi-level pinning at the charge neutrality level (CNL), which is very close to the valence band. The CNL

of Ge and Si are calculated to be 0.03 and 0.23 eV above the valence band respectively.[22] Both are located at the lower half of the band gap. The position of the CNL is an additional factor that can explain the SBH asymmetry between n- and p-type Si observed in our case and in many other studies.

All the factors mentioned above contribute to the overall final band bending near the interface, which leads to the SBH behaviors observed for the different monolayers and types of substrates.

Finally, regarding the generally observed trend for a lower SBH for the oxygen-rich interfaces, we note that a few samples do not follow this trend. Specifically, these are Er and Al for p-type. Further studies are necessary to elucidate the causes of these observations.

4. Conclusions

In this work, we have studied the impact of the surface treatments on the SBH modulation of metal/MgO/Si stacks. Mg or O rich interface layers have been selectively deposited as the first monolayers. The nominal thickness of MgO is 0.5 nm for all studies. Different metal contacts (Er, Al, Au, and Pt) have been employed in the stacks. The SBH increases (decreases) with increasing metal work function for n-type (p-type). For Er and Au on n-Si, the barrier height of the MOS stack using the O-first MgO layer is more than 0.1 eV lower than that of MgO or Mg-first layer. In the case of p-Si, Fermi-level pining is evidently observed and complicates the SBH study.

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